

Search Report

STIC Database Tracking Number 26257

To: HIEN NGUYEN Location: JEF-7D15

Art Unit: 2824

Thursday, June 05, 2008

Case Serial Number: 09/783,183

From: DIANE JACKSON

Location: EIC2800 JEF-4B68 / JEF-4B68 Phone: (571)272-3260

diane.jackson@uspto.gov

Search Notes

Attached are litigation search results in Lexis Nexis, and CourtLink and Questel-Orbit.

No Litigation was found for Serial Number 09/783183.

If you have any questions, please feel free to contact me.

Thanks,

Diane





Selected file: PLUSPAT

PLUSPAT - (c) Questel , All Rights Reserved.
RELOADED 02/2008 Comprehensive Worldwide Patents database
Individual records for each Country or Patent Office
Coverage: 78 patenting authorities; start dates vary from 1800 forward
Abstracts/Titles in English , French & German. Increased
standardization
of Assignee/Inventor names. Added cited ref's BE , CH , NL , TR , AU ,
& JPB
For PlusPat Fact Sheet , Pricing and FAQ , see the Questel website
Last update of file: 2008/05/30 (YYYY/MM/DD) 2008-22/UP (last update)

Search statement 1

nbr/pn us6166952

PLUSPAT1 US6166949	*			1
PLUSPAT2 US616695				1
PLUSPAT3 US6166950		•		1
PLUSPAT4 US6166951				. 1
PLUSPAT5 US6166952			•	1
PLUSPAT6 US6166953				1
PLUSPAT7 US6166954		•		1
PLUSPAT8 US6166955		•		1
PLUSPAT9 US6166956				1
PLUSPAT10US6166957	•		•	. 1
PLUSPAT11US6166958		•		1
PLUSPAT12US6166959				1
PLUSPAT13US616696				1
PLUSPAT14US6166960				1
PLUSPAT15US6166961				1
Some: numbers / Continue	: Y / None:	N		

Search 1 - 5 - 1

** SS 1: Results 1

Continue: Y / N

prt full legalall max

Select All | Unselect All

1/1 PLUSPAT - Worldwide Patents - ©Questel



US6166952 (A) Read-only memory having specially output circuits and word line connected...

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US6166952 A 20001226 [US6166952]
PN
      (A) Read-only memory having specially output circuits and word line
TI
      connected to a group of memory cells
      (A) INFINEON TECHNOLOGIES AG (DE).
PA
      Infineon Technologies AG, Munich [DE]
PA0
IN
      (A) SEDLAK HOLGER (DE)
      US9357398 19980608 [1998US-0093573]
AP
FD
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      DE19545557 19951206 [1995DE-1045557]
PR
      WODE9602241 19961121 [1996WO-DE02241]
IC
      (A) G11C-016/04
      G11C-016/04 [2006-01 A - IR M EP]
ICAA
      G11C-017/12 [2006-01 A - I R M EP]
      G11C-016/04 [2006 C - I R M EP]
ICCA
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      G11C-016/04F1
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      ORIGINAL (O): 365185050; CROSS-REFERENCE (X): 365185180
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      US5065364 [US5065364] 365185000
      -US5249158 [US5249158] 365230030
       -US5267196 [US5267196] 365185000
       -US5337281 [US5337281] 365218000
      -US5687117 [US5687117] 365185120
      -US5768194 [US5768194] 365185330
       -US5825688 [US5825688] 365185110
CT
       -US5945717 [US5945717] 257390000
      -US5963478 [US5963478] 365185290
       -EP0509184 Z1 [EP-509184]
       -EP0561271 A2 [EP-561271]
       -EP0627742 A2 [EP-627742]
      -EP0637035 A1 [EP-637035]
       -Patent Abstracts of Japan No. 5-28783 (Yamamoto), dated Jul. 24, 1991.
STG
      (A) United States patent
       A read-only memory having a multiplicity of memory cells whose contents
       can be read out with appropriate addressing by word, bit and source lines.
       The read-only memory is distinguished by the fact that the memory cells
AB
       which can be addressed via an individual word line are divided into a
       multiplicity of groups, to each of which a separate common source line is
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assigned. Accordingly, a group-by-group read-out of the memory cells which

can be addressed via an individual word line is carried out.

UP 2001-03

1/1 LGST - Legal

Status - ©EPO

US6166952 20000710 US/ASAASSIGNMENTOWNER: SIEMENS

AKTIENGESELLSCHAFT ZT GG VM POSTFACH...

PN US6166952 A 20001226 [US6166952]

AP US9357398 19980608 [1998US-0093573]

20000710 US/AS-A

ASSIGNMENT

OWNER: SIEMENS AKTIENGESELLSCHAFT ZT GG VM POSTFACH

22 16; EFFECTIVE DATE: 19980630

ACT ASSIGNMENT OF ASSIGNORS INTEREST; ASSIGNOR: SEDLAK,

HOLGER;REEL/FRAME:010954/0986

20030909 US/RF-A

REISSUE APPLICATION FILED

EFFECTIVE DATE: 20010214

UP 2004-29

☐ 1/1 CRXX - US Claims

Reassignations - ©CLAIMS/RRX

US6166952 20010214 REISSUE REQUESTEDISSUE DATE OF O.G.: 20030909REISSUE REQUEST NUMBER...

AN 3438618

PN 6,166,952 A 20001226 [US6166952]

PA Infineon Technologies AG DE

PT E (Electrical)

20010214 REISSUE REQUESTED ISSUE DATE OF O.G.: 20030909

REISSUE REQUEST NUMBER: 09/783183

ACT EXAMINATION GROUP RESPONSIBLE FOR REISSUEPROCESS: 2824

Reissue Patent Number:

UP 2003-37. UACT 2003-09-09

Search statement

Selected file: FAMPAT

FAMPAT - (c) Questel , All Rights Reserved. RELOADED 02/2008 Searchable bibliographic & abstracts-all family members

Search & display options for both FamPat & extended family definition Coverage: 78 patenting authorities; start dates vary from 1800 forward Abstracts/Titles in English , French & German. Increased standardization

of Assignee/Inventor names. Added cited ref's BE , CH , NL , TR , AU , & JPB

For more details , see the FamPat Fact Sheet and Questel website Last update of file: 2008/05/30 (YYYY/MM/DD) 2008-22/UP (last update)

Search statement 1

nbr/pn us6166952

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So	ome: numbers / Continue: Y / None: N		

Search 1 - 5 - 1

** SS 1: Results 1

Continue: Y / N

prt full legalall max

Select All | Unselect All

1/1 FAMPAT - Patent Families - ©Questel

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DE19545557 READ-ONLY MEMORY AND METHOD OF COMMANDING
SAME
FAN
     20042781480118
        DE19545557 A1 19970612 [DE19545557]
                    A2 19970612 [WO9721225]
        WO9721225
        WO9721225
                    A3 19970814 [WO9721225]
        EP0882294
                    A2 19981209 [EP-882294]
                    A 19981230 [CN1203687]
        CN1203687
        JP2000501221 T 20000202 [JP2000501221]
        EP0882294
                    B1 20000308 [EP-882294]
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                    T 20000315 [ATE190427]
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        ES2144284
                    A 20001226 [US6166952]
        US6166952
                    C2 20021010 [RU2190885]
        RU2190885
        CN1106646
                    C 20030423 [CN1106646C]
                    A1 20030809 [IN-190574]
        IN190574
ΤI
      READ-ONLY MEMORY AND METHOD OF COMMANDING SAME
      INFINEON TECHNOLOGIES AG
      SEDLAK HOLGER
PA
      SIEMENS AG
      SIEMENS AKTIENGESELLSCHAFT; Wittelsbacherplatz 2; 80333
PA0
      München (DE)
IN
      SEDLAK HOLGER
      1995DE-1045557 19951206
      1998RU-0112272 19961121
      1996ES-0945894 19961121
      1996DE-5004631 19961121
      1996JP-0520857 19961121
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      1996CN-0198868 19961121
      1996WO-DE02241 19961121
      1996EP-0945894 19961121
      1996IN-CA02090 19961204
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      G11C-016/04
      G11C-016/06
IC
      G11C-017/08
      G11C-017/12
      G11C-017/14
      G11C-017/18
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      G11C-016/06 [2006-01 A L I R M JP]
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      G11C-017/18 [2006-01 A L I R M JP]
      G11C-016/04 [2006 C - I R M EP]
      G11C-016/06 [2006 C L I R M JP]
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      G11C-017/14 [2006 C L I R M JP]
      G11C-016/04F1
EC
      G11C-017/12
      ORIGINAL (O): 365185050; CROSS-REFERENCE (X): 365185180
PCL
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DS
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      (WO9721225)
      CN JP KR RU UA US
DS
      European patent: AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL
      PT SE
      (EP-882294)
CT
      Cited in the search report
      -See references of WO 9721225A2
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-EP0627742 A2 [EP-627742]
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-EP0637035 A1 [EP-637035]

-Patent Abstracts of Japan No. 5-28783 (Yamamoto), dated Jul. 24, 1991. (WO9721225)

Cited in the search report

-EP0637035(A1)(Cat. X)[EP-637035]

CT -EP0509184(A1)(Cat. X)[EP-509184]

-US5267196(A)(Cat. X)[US5267196]

-US5249158(A)(Cat. A)[US5249158]

-EP0561271(A2)(Cat. A)[EP-561271]

(DE19545557)

Cited in the search report

-US5337281(A)[US5337281]

-US5065364(A)[US5065364]

-JP 5-28783 A. In: Patents Abstracts of Japan, P-1557, Vol. 17, No. 314, 15.6.93

(US6166952)

A read-only memory having a multiplicity of memory cells whose contents can be read out with appropriate addressing by word, bit and source lines. The read-only memory is distinguished by the fact that the memory cells which can be addressed via an individual word line are divided into a multiplicity of groups, to each of which a separate common source line is

assigned. Accordingly, a group-by-group read-out of the memory cells which can be addressed via an individual word line is carried out.

(US6166952)

The present invention relates to a read-only memory which has a multiplicity of memory cells whose contents can be read out with appropriate addressing by word, bit and source lines.

It is accordingly an object of the invention to provide a read-only memory and method for addressing the same which overcome the hereinafore-mentioned disadvantages of the heretofore-known products and methods of this general type, and where the reading out of data from the ROM can be carried out faster and with a reduced power consumption.

With the foregoing and other objects in view there is provided, in accordance with the invention, a read-only memory, including word lines, bit lines and source lines, each of the bit lines having a bit line potential; a multiplicity of memory cells connected to the word lines, the bit lines and the source lines, the memory cells having data contents and the data contents are read out with appropriate addressing of the word lines, the bit lines and the source lines, the memory cells are addressed by an individual word line; the memory cells are divided into a multiplicity of memory cell groups, each of the memory cell groups has a separate common source line, the memory cell groups forming a memory cell array; common data output lines; and connecting devices connected between the bit lines of the memory cells of the memory cell groups and the common data output lines for outputting the data contents stored in the memory cells, the connecting devices operating

OBJ

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under sole dependency on the bit line potential.

With the foregoing and other objects in view there is also provided, in accordance with the invention, a method for addressing a read-only memory having a multiplicity of memory cells storing data, word lines, bit lines, source lines, and common data output lines, the memory cells being divided into a multiplicity of memory cell groups, each of the memory cell groups having a separate common source line and the memory cell groups forming a memory cell array being addressed by the word lines, the bit lines and the source lines, which includes carrying out a group-by-group read-out of the memory cells being addressed via an individual word line. (US6166952)

Each of the groups have a separate common source line, and group-by-group reading out of the memory cells which can be addressed via an individual word line are carried out.

These measures make it possible to address, for the purpose of reading out, and only those memory cells whose contents are actually intended to be outputted from the read-only memory.

This limited or partial reading capability has not been previously possible to date on account of the provision of only a single common source line for all the memory cells of the memory cell array (the discharge of the precharged bit lines could only take place in units of rows of the memory cell array). (US6166952)

1. A read-only memory, comprising:

word lines, bit lines and source lines, each of said bit lines having a bit line potential;

a multiplicity of memory cells connected to said word lines, said bit lines and said source lines, said memory cells having data contents and the data contents being read out with appropriate addressing of said word lines, said bit lines and said source lines, said memory cells addressed by an individual word line;

said memory cells divided into a multiplicity of memory cell groups, each of said memory cell groups having a separate common source line, said memory cell groups forming a memory cell array;

ICLM common data output lines, each memory cell group connected to a respective one of said common data output lines; and

connecting devices connected between said bit lines of said memory cells of said memory cell groups and said common data output lines for outputting the data contents stored in said memory cells, each of said connecting devices for putting a potential that is on one of said bit lines onto one of said common data output lines at the beginning of a read cycle while said one bit line is discharging and for subsequently actively driving said one bit line.

18. A connection configuration, comprising:

a bus line and a bit line;

switches connected to a precharge line, said switches for switching said bus line to a first potential and said bit line to a second potential; holding elements for holding potentials on said bit line and on said bus line,

when said bit line and said bus line have been precharged; and a further switch connected to said bit line for switching said bit line to a source line at said first potential and for switching said bus line to said second potential, when said bit line has been connected to the source line atsaid first potential.

UP 2000-08

1/6 LGST - Legal Status - ©EPO

· US6166952 20000710 US/ASAASSIGNMENTOWNER: SIEMENS

AKTIENGESELLSCHAFT ZT GG VM POSTFACH...

PN US6166952 A 20001226 [US6166952]

AP US9357398 19980608 [1998US-0093573]

20000710 US/AS-A

ASSIGNMENT

OWNER: SIEMENS AKTIENGESELLSCHAFT ZT GG VM POSTFACH

22 16; EFFECTIVE DATE: 19980630

ACT ASSIGNMENT OF ASSIGNORS INTEREST; ASSIGNOR: SEDLAK,

HOLGER;REEL/FRAME:010954/0986

20030909 US/RF-A

REISSUE APPLICATION FILED

EFFECTIVE DATE: 20010214

UP 2004-29

2/6 LGST - Legal Status - ©EPO

ES2144284 20000601 ES/FG2ATDEFINITIVE PROTECTIONPROTECCION DEFINITIVA(EP 882294 [EP88...

PN ES2144284 T3 20000601 [ES2144284]

AP ES96945894T 19961121 [1996ES-0945894]

20000601 ES/FG2A-T

ACT DEFINITIVE PROTECTION PROTECCION DEFINITIVA (EP 882294 - [EP-882294])

UP 2003-22

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Status - ©EPO

WO9721225 19970612 WO/AK [+]DESIGNATED STATES CITED IN A SUBSEQUENTLY PUBLISHED SEARC...

PN

WO9721225 A2 19970612 [WO9721225]

WO9721225 A3 19970814 [WO9721225]

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WODE9602241 19961121 [1996WO-DE02241]

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SEARCH REPORT

CN JP KR RU UA US

19970612 WO/AL [+]

DESIGNATED COUNTRIES FOR REGIONAL PATENTS CITED IN A

SUBSEQUENTLY PUBLISHED SEARCH REPORT

AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE

19970807 WO/DFPE

REQUEST FOR PRELIMINARY EXAMINATION FILED PRIOR TO

EXPIRATION OF 19TH MONTH FROM PRIORITY DATE

19970814 WO/AK [+]

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CN JP KR RU UA US

19970814 WO/AL [+]

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SUBSEQUENTLY PUBLISHED SEARCH REPORT

AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE

19970910 WO/121

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EP: THE EPO HAS BEEN INFORMED BY WIPO THAT EP WAS

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20030521 WO/WWG [+]

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UP 2008-18

4/6 LGST-Legal

Status - ©EPO

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PN DE59604631 D1 20000413 [DE59604631]

AP DE59604631 19961121 [1996DE-5004631] 20010329 DE/8364-A [+]

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UP 2003-22

5/6 LGST - Legal

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Status - ©EPO

DE19545557 19970612 DE/OP8A [+]REQUEST FOR EXAMINATION AS TO PARAGRAPH 44 PATENT LAWPR...

PN DE19545557 A1 19970612 [DE19545557]

AP DE19545557 19951206 [1995DE-1045557]

19970612 DE/OP8-A [+]

REQUEST FOR EXAMINATION AS TO PARAGRAPH 44 PATENT LAW

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WITHDRAWAL

ZURUECKNAHME

UP 2003-22

6/6 LGST - Legal

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Status - ©EPO

EP-882294 19981209 EP/AKA [+]DESIGNATED CONTRACTING

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EP0882294 A2 19981209 [EP-882294] PN

EP0882294 B1 20000308 [EP-882294]

EP96945894 19961121 [1996EP-0945894] AP

19981209 EP/AK-A [+]

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AT CH DE ES FR GB IT LI

19981209 EP/17P-A [+]

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PRUEFUNGSANTRAG GESTELLT

EFFECTIVE DATE: 19980519

19990120 EP/17Q-A [+]

FIRST EXAMINATION REPORT

ERSTER PRUEFUNGSBESCHEID

EFFECTIVE DATE: 19981208

20000308 EP/AK-A [+]

DESIGNATED CONTRACTING STATES:

BENANNTE VERTRAGSSTAATEN

AT CH DE ES FR GB IT LI

20000308 EP/REF-A

CORRESPONDS TO:

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(AT 190427T 20000315 [ATE190427])

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20000315 EP/REG-A; CH/NV

CH: NEW AGENT

CH: NEUER VERTRETER/NOUVEAUX MANDATAIRES/NUOVI

MANDATARI

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REPRESENTATIVE: SIEMENS SCHWEIZ AG

20000413 EP/REF-A

CORRESPONDS TO:

ENTSPRICHT

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20000530 EP/ITF-A [+]

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IT: DEPOSITO TRADUZIONE DI BREVETTO EUROPEO

OWNER: STUDIO JAUMANN P. & C. S.N.C.

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ES: DEFINITIVE PROTECTION

ES: PROTECCION DEFINITIVA

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77(6)(A)/1977)

GB: TRANSLATION OF EP PATENT FILED (GB SECT. 77(6)(A)/1977)

EFFECTIVE DATE: 20000512

20000713 EP/ET-A [+]

FR: TRANSLATION FILED

FR: TRADUCTION A ETE REMISE

20010221 EP/26N-A [+]

NO OPPOSITION FILED

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20031120 EP/PGFP-A [+]

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CH: LOESCHUNG/RADIATION/RADIAZION

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PAYMENT DATE: 20061127; PAYMENT YEAR: 11

20070115 EP/PGFP-A [+]

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PAYMENT DATE: 20071116; PAYMENT YEAR: 12

20080430 EP/PGFP-A [+]

POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE

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PAYMENT DATE: 20071122; PAYMENT YEAR: 12

20080430 EP/PGFP-A [+]

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PAYMENT DATE: 20071120; PAYMENT YEAR: 12

UP 2008-20

1/1 CRXX - US Claims
Reassignations - ©CLAIMS/RRX

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AN 3438618

PN 6,166,952 A 20001226 [US6166952]

PA Infineon Technologies AG DE

PT E (Electrical)

20010214 REISSUE REQUESTED ISSUE DATE OF O.G.: 20030909

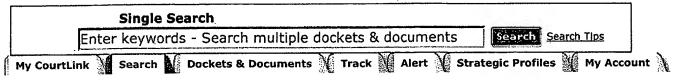
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December 26, 2000

Read-only memory having specially output circuits and word line connected to a group of memory cells

REISSUE: February 14, 2001 - Reissue Application filed Ex. Gp.: 2824; Re. S.N. 09/783,183 (O.G. September 9, 2003)

INVENTOR: Sedlak, Holger - Munchen, Germany (DE)

APPL-NO: 093573 (09)

FILED-DATE: June 8, 1998

GRANTED-DATE: December 26, 2000

PRIORITY: December 6, 1995 - 19545557, Germany (DE)

ASSIGNEE-PRE-ISSUE: July 10, 2000 - ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS)., SIEMENS AKTIENGESELLSCHAFT ZT GG VM POSTFACH 22 16 34MUNCHEN, (1)80506, Reel and

Frame Number: 010954/0986

ASSIGNEE-AT-ISSUE: Infineon Technologies AG, Munich, Germany (DE), Foreign company or corporation

(03)

LEGAL-REP: Lerner, Herbert L.; Greenberg, Laurence A.; Stemer, Werner H.

PUB-TYPE: December 26, 2000 - Utility Patent having no previously published pre-grant publication (A)

PUB-COUNTRY: United States (US)

REL-DATA:

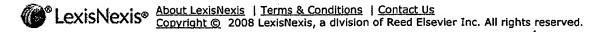
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US-MAIN-CL: 365#185.05

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